Is Now the Time for Reconfigurable Computing Standards?

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Outline

- Motivation: future systems requirements

- Status: Reconfigurable Computing (RC)
  - barriers and challenges
  - strategic directions for RC R&D in Europe (FP7 funding)

- Standards:
  - benefits, learning from other communities
  - OpenFPGA standardization activities
My Personal History of Reconfigurable Computing

- **Cray XD1**
  - 6x VIIPro50, RapidArray

- **Nallatech H101**
  - 2x V4LX120, PCI-X

- **SGI Altix450**
  - 2x RC100, 2xV4LX200, NL

- **Mitrionics SDK**
  - v. 0.9 ... v. 2.0.x
Some Observations and Trends

- Resource provider are in strong competition to support science
  - computational & storage requirements
  - power/cooling issues continue to grow

- RC vendors -- changes happen ...
  - Convey entered / SRC, Nallatech, ... continue / Cray, SGI left RC field
  - impact on sustainability from user‘s/developer‘s point of view

- GPGPU gain traction on x86
  - A likely convergence of GPU and CPU elements in future processors?
    - see yesterdays talk by Norm Rubin
Recap: (Some) Attributes of Architecture of the Future

- **scalability** at Exascale level

- **investment and operational costs**
  - reduced cost per solution
    - use of consumer market technologies
  - application performance efficiency \(\rightarrow\) specific targeted solutions
    - adaptive / heterogeneous computing
    - low power + high efficiency
    - embedded and low-power ideas from mobile devices

- **built-in redundancy for fault tolerance**
Example: **Green Flash** feasibility study at LBNL
- application target is climate modeling
- goal to influence HPC design
- design for low power and greater concurrency
- lower clock rates
- simpler cores (Tensilica SoC)
- **tailor design to application**

*source: Horst Simon, April 2009*
Top Barriers to RC Supercomputing

1. Programming (languages and models, ease of programming)
2. Standards (communications, heterogeneous interconnection, interfaces, portability)
3. Tools
4. Education
5. Costs
6. Development time

source: OpenFPGA survey, November 2009
Additional Barriers to Sustainable RC

- other barriers mentioned in survey
  - Technical
    - memory size and speed
    - bandwidth between FPGA and general-purpose front end
    - high level languages to HDL
  - Non-technical
    - software
    - availability, license costs
    - robust codes for end-users
  - Personnel
    - productivity

source: OpenFPGA survey, November 2009
RC Challenges Associated with Missing Standard

- mainstream RC applications take significant effort to create
- developments not portable across products and time
- industry is fragmented
  - run-time and programming environments: embedded vs. non-embedded
  - businesses: big and focused, small and niche
- alternative technologies in accelerator market
  - low-power processors, GPGPU, multi-core, and combinations
  - better and less expensive tool chains
  - rapidly growing communities
  - standards: OpenCL
Reconfigurable Supercomputing Today

- Are FPGAs dead?
  - Will CPUs solve all problems?
  - Will GPUs fill in the gaps?
  - Will performance continue to matter?

- FPGAs are not dead...
  - parallel processing wall will force code and system redesign
    - applies for GPGPU, FPGA, multi-core
  - data volumes are growing and FPGAs are very efficient at data processing
  - power efficiency is increasingly important
  - FPGAs are growing in capability per unit cost

The door remains open for reconfigurable supercomputing
What’s Ahead for Reconfigurable Computing

Gartner Group Technology Adoption Cycle
RC within EU PRACE Project

- 2009: SRC and Convey are listed as RC platforms of interest

- 03/2010: existing RC prototype for evaluation:
  - HW: MAXWELL FPGA cluster (EPCC)
  - SW: HCE (C-to-HDL/Ylichron)

- 06/2010: the RC prototype was excluded from further benchmarking activities (so far)

source: http://www.prace-project.eu/documents/
EU FP7 Funding Opportunities ICT - Call #7 in 09/2010

- Objectives: ..., Customisation
  - Reconfigurable architectures
  - Tool-chains

- EU strengths:
  - academic (& some industrial) research, coarse-grained RC research
  - embedded systems (as a potential market)

- R&D in Reconfigurable Computing must take account of the market:
  - principal markets:
    - High Performance Computing
    - Embedded Systems
  - fundamental obstacle to take-up (in both) is difficulty of programming
  - highest priority need is for commercially viable programmability

source: P. Tsarchopoulos, ICT Programme Officer, DATE 2010
Benefits of Standards

- increase lifetime of created products
- lower risk of new innovations
- increase confidence of consumers
- encourage interoperability
- enable markets to expand

- several standards exist in the RC hardware design community already
Reaching for Standards

- must build value
  - Business: reduced cost and/or expanded markets
  - Education: foster innovation, research and learning
- must be correctly timed
  - enable, not stifle innovation that is of market value
- must be adoptable
  - low cost to incorporate
- must be adaptable
  - there is no perfect standard

- How to reach standards?
  - Learning from history - Do we need a (RC) crisis?
Learning from GPU Community

- crisis driven: x86 lock speeds were performance needed
- reduce costs of tools to create applications
  - CUDA is available for free
  - free/inexpensive OpenCL compiler
- expansion opportunity: inexpensive devices for development
  - GPUs are cheap to develop with
- shorten time to develop applications
  - short cycle times
  - solutions could be readily used on other compatible devices
- grow the number of reliable applications
  - efforts abound with increasing numbers of enhanced applications and libraries
OpenFPGA & Standards

- recognizing and promoting progress in standards for RC computing internationally
- OpenFPGA is not ‘open source’
  - OpenCores fills this important niche for the market
- OpenFPGA seeks to extend life of intellectual property
  - standards and metadata
- OpenFPGA seeks to translate research advances into broader mainstream use
  - for example, developments in CHREC
- OpenFPGA seeks to ease programmability
  - increased reliability
  - increased reusability
  - better inter-operability
OpenFPGA Working Groups

- **T-HLLANG**
- **T-GENAPI**
- **T-CORELIB**
- **T-APPLIB**

**Performance**

**T-BENCH**

**Functional Abstractions**

**Control and Flow Interfaces**

**Component Reliability and Reuse**

FPGA ENABLED SYSTEM
OpenFPGA Activities Towards Standards

- Core interface definition (2007)
- GenAPI (2008)

- OpenFPGA member activities:
  OpenCL (“like”) interface on FPGA platforms, for example...
  → see poster of Craig Steffens (NCSA)
OpenFPGA CoreLib Interoperability Effort (2007-)

1. Investigate emerging standards for IP cores.
2. Select an existing standard if possible → Spirit consortium IP-XACT
3. Investigate existing HLL tools requirements for IP core integration. Integrate a set of examples into each of the tools.
4. Define extensions required to existing standards to meet needs of HLL tools → OpenFPGA IP-XACT extensions
5. Define the core standard and implement it in the tools.
6. Define the library standard.
7. Select and implement example IP core libraries.
OpenFPGA GenAPI (2008)

- API for high-level language access to RC resources in a portable manner
- Design goals:
  - Portability and supportability across a wide range of available RC platforms
  - Similarity to existing common capabilities available within RC platforms
  - Minimal essential functionality to support general application acceleration with RC
- early API defined July 2008 and released for comment
  - available at OpenFPGA website
- comment being received slowly
- awaiting proof case incorporation
Open Discussion (➔ OpenFPGA Meeting)

- What is the future if RC standards are not adopted?
- What will drive RC supercomputing towards standards?
- Decision or challenge about which way to go?
- Who would like standards?
  - If so, what standards?
  - If not, why not?