40Gbps+ Full Line Rate, Programmable Network Accelerators for Low Latency Applications

SAAHPC
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www.nallatech.com
**Company Overview**

**ISI + Nallatech + Innovative Integration**

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Sales by Solution Type

FPGA Products
- High Performance FPGA Products, 30%
- 3D, Multi-Chip Modules & Bare-Die Assemblies, 30%
- IC Adapters & Obsolescence Solutions, 20%
- Interconnect & Reballing, 20%

ISI Products

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Nallatech’s Emerging Product Focus

» Near Sensor Processing
» ISI & Nallatech Combined
» Distributed Computing
  » Move Processor not the data
» SWaP Critical Applications

» Programmable Network Accelerators
» Ethernet Focused
» 1GbE, 10GbE, 40GbE Today
» 100GbE Planning
» PCIe Card based

System Level Compatibility
Programmable Network Accelerator Applications

» Adaptive Optics
» Deep Packet Inspection, DPI
  » Intrusion detection Systems IDS
  » Data Filtering
  » Content Management & Billing
  » “Kink in the Wire” Packet monitoring and modification
» Financial Trading
» Improving Network Efficiency - e.g. Compression
» Improving Network Security – e.g. Encryption
» Distributed Computing – Data Reduction
» Unobtrusive Network Monitoring
Detecting exoplanets using ground-based telescopes is especially challenging since the light you are sampling is constantly being distorted by Earth’s atmosphere.

Adaptive Optics (AO) provides a means of compensating for atmospheric turbulence.
Deep Packet Inspection – Aho-Corasick method

» Effectively a Mealy finite state machine
  » Next State = func{input & current state}

» Implemented in SRAM Memory
  » Depth primarily determined by size of dictionary
  » Random look up & Low Latency are critical to performance & efficiency

» Trivial amount of Compute required
The Challenge – Full Line Rate DPI Network Processing – 10GbE example – 2009 vintage

» Aho-Corasick String Matching Operations at Full Line Rate
   » Large Random, low latency LUT required using external SRAMs
   » Analyze ALL data, not just Metadata
   » A 10Gb/s Network Card requires 1.25GLookups/s random access rates to memory
      » Random lookup rate to DDR3 SDRAM <50MLookups/s
      » Random Lookup rate of DDR2 SSRAM >250MLookups/s
   » Xeon too powerful a CPU and too poor at random system memory access

» Store & Retrieve Network data at full Line rate
   » Delay messages for later retrieval after search complete
   » SDRAM capable of storing up to 100’s of milliseconds of data.
   » 2x Line Rate for simultaneous writes of new data and reading of old data
   » 2x line rate = 2.5GByte/s
   » 250MHz DDR2 x72 peak access rate = 250 x2 x8 = 4GByte/s
Perfectly Balanced 10GbE DPI Network Accelerator

- Aggressive Performance/$
  - Starts at $2000 for 1K units quantities
- Optimum Form Factor
  - Low profile (half length, half height)
  - 8-lane PCI Express 1.1
- 10GbE sources & Sinks 1.25GBytes/s of data
  - Supports LAN & WAN
- Host Interface Supports Full line rate read & write
  - 1.3 GB/s WRITE (system to card)
  - 1.3 GB/s READ
- SRAM Supports Full Line Rate Random Lookup
  - Five independent banks (40MBytes total)
  - Total memory bandwidth of 10GBytes/sec
  - 1.25Gbytes/s random read rate
- SDRAM Supports Full Line Rate Read & Write
  - 512MBytes of DDR2 SDRAM
  - Memory bandwidth of 4GBytes/sec
- Scalable Processing
  - Supports Xilinx Virtex-5 LX100 to LX155 FPGA
The Full Line Rate DPI Dataflow

AC = Aho-Corasick Engine
10GbE Programmable Network Accelerator Appliance

1U Hybrid Computing Platforms

» IBM Server Support
» PCIe-180 FPGA card
» Finnisar Optical Transceiver
» Reference Design
» Integration, Support and Warranty services
Adding Programmability to the Network Accelerator

» An Accelerator that just works out of the box
  » Acts as a standard NIC

» Click & go acceleration options
  » E.g. GZIP and AES
  » Host driver configurable

» Add Custom Accelerator
  » VHDL or DIME-C

» Protocol Light Network Options
  » Reduced Latency
  » E.g. Direct connect to Nallatech NSP Products
PCle-287N – 1GbE, 10GbE & 40GbE Implementation

PCle-287N
PCI-Express Network Processor Solution

» 4x 1GbE/10GbE or 2x 40GbE ports
» Maintain Full Line Rate DPI of 4x 1GbE and 2x 10Gbe channels
» Support Full Line Rate DPI of Metadata for 2x 40GbE channels
» Comprehensive application development support
  » Simplifying Programmability
Full Line Rate processing for 100GbE

» Aho-Corasic needs 12.5GByte/s Random Lookup rate
  » Equivalent to 50x DDR2-SSRAM chips at 250MHz
» Sustained DDR3 DRAM Bandwidth of 25GBytes/s
  » Read & Write 100Gb data simultaneously
  » Equivalent to 7x 250MHz DDR2 DIMMS

2009 Technology
Moores Law = 2.5 cards in 2012
Potential Memory Performance with 28nM FPGAs

» Typically support up to 6 banks of DDR3 Memory
  » 1600MTPS to 1866MTPS interface speeds
  » Tight coupling with ISI Memory Modules

» New Pseudo SSRAM Technology
  » Significant Performance & density improvements

» 120GB/s achievable external aggregate memory bandwidth per FPGA
  » Approaching GPU External Memory bandwidths

» For Aho-Corasic
  » Delivers ½ of required Random Access Bandwidth
  » Deliver 3x the DDR3 Memory Bandwidth
Summary

» FPGAs Have a critical role to play in HPC systems
» Increasingly Careful Memory management is critical to Compute performance
  » Align processing with dataflow
  » FPGAs are the ideal pipeline dataflow processors
» Network interface ideal point for FPGA Acceleration
» Make the Accelerator Transparent to the User
Thank you

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