Addressing the Increasing Challenges of Debugging on Accelerated HPC Systems

2012 Symposium on Application Accelerators in High-Performance Computing (SAAHPC'12)

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Senior Sales Engineer

Agenda

- Overview - Rogue Wave & TotalView
- GPU Debugging with TotalView
  - Nvdia CUDA
  - Intel Phi

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Rogue Wave Today

ROGUE WAVE® SOFTWARE

The largest independent provider of cross-platform software development tools and embedded components for the next generation of HPC applications

Visual Numerics®

Leader in embeddable math and statistics algorithms and visualization software for data-intensive applications.

Leading provider of intelligent software technology which analyzes and optimizes computing performance in single and multi-core environments.

Industry-leading interactive analysis and debugging tools for the world's most sophisticated software applications.

Latest addition to the Rogue Wave family: **Rogue Wave Visualization for C++**
(Formerly IBM's ILOG Visualization for C++ products)

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Representative Customers

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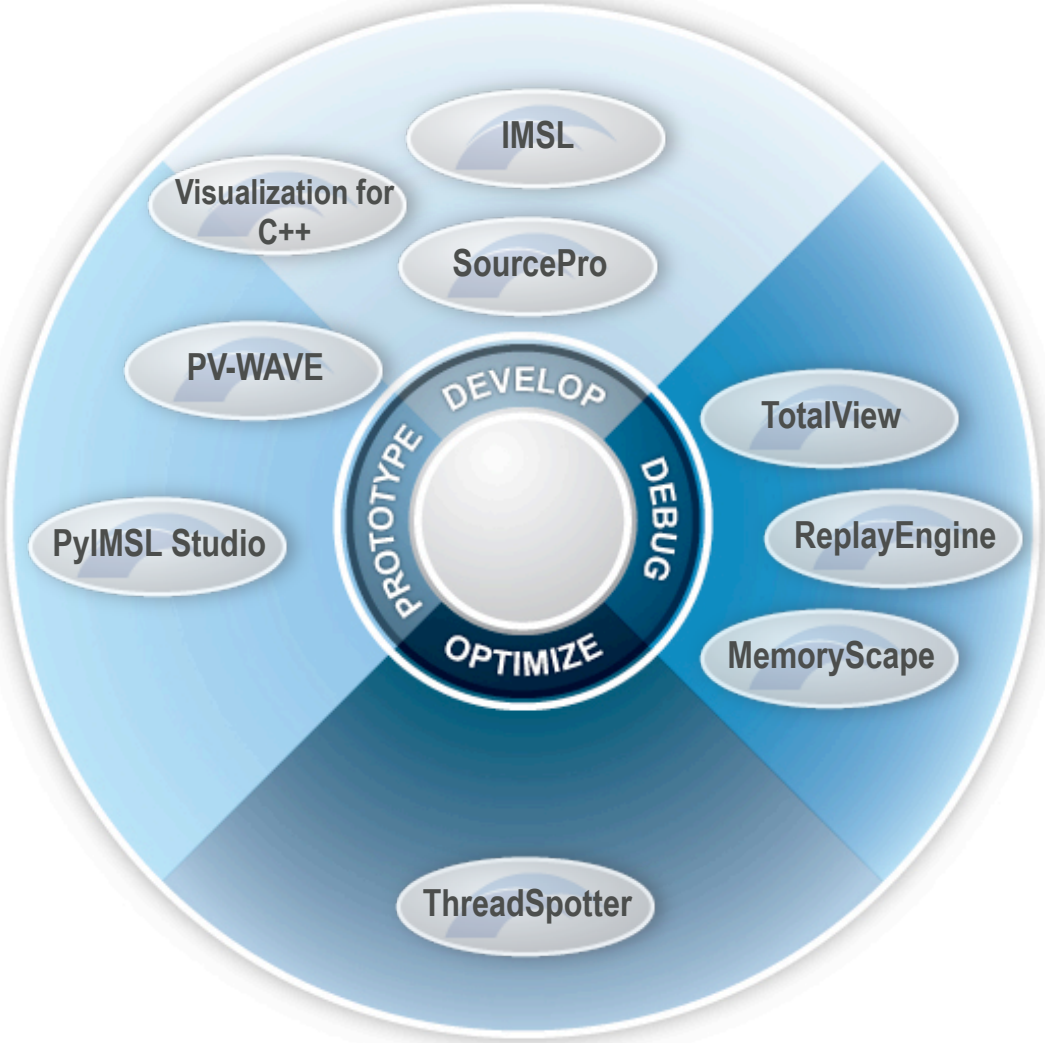
Rogue Wave Product Offerings



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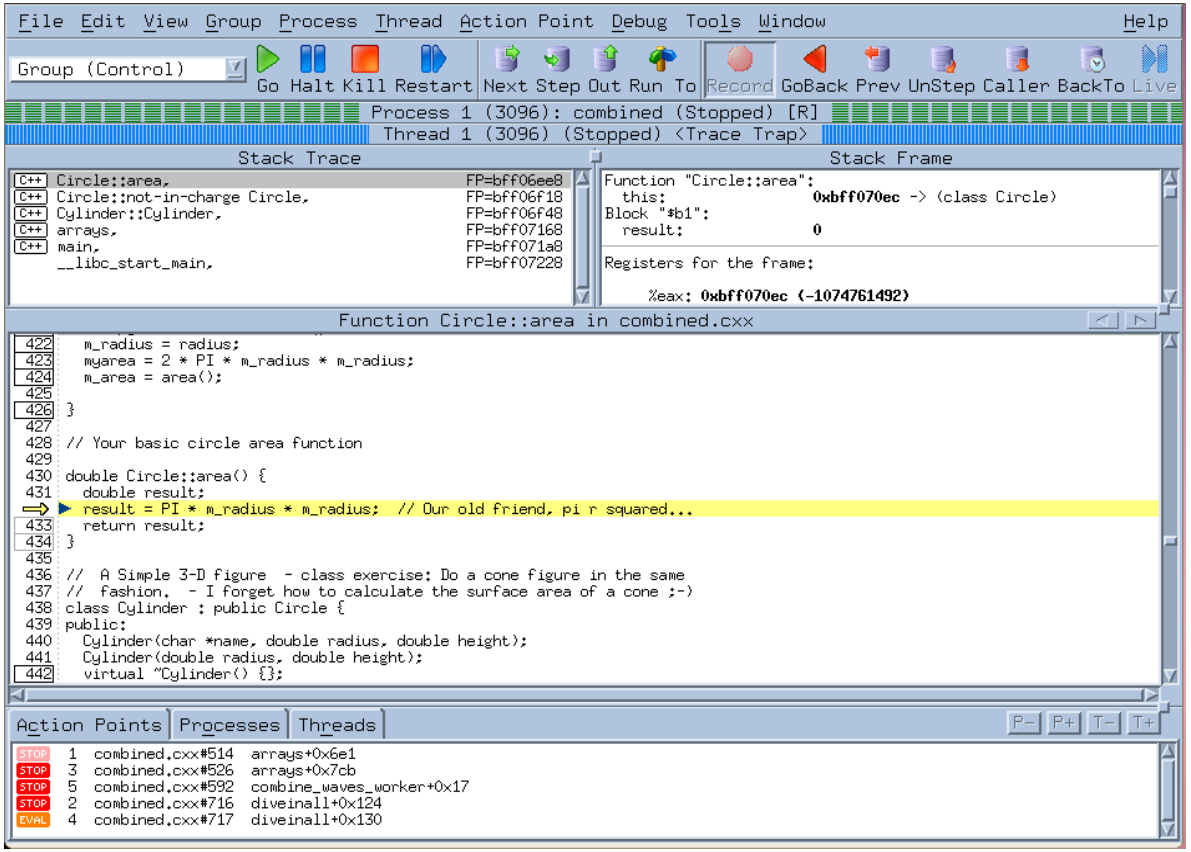
What is TotalView?

A comprehensive debugging solution for demanding parallel and multi-core applications

- **Wide compiler & platform support**
  - C, C++, Fortran 77 & 90, UPC
  - Unix, Linux, OS X
- **Handles Concurrency**
  - Multi-threaded Debugging
  - Multi-process Debugging
- **Heterogeneous Systems Support**
- **Integrated Memory Debugging**
- **Reverse Debugging for Linux**
- **Supports Multiple Usage Models**
  - Powerful and Easy GUI – Highly Graphical
  - CLI for Scripting
  - Long Distance Remote Debugging
  - Unattended Batch Debugging



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GPU Debugging

with

TotalView

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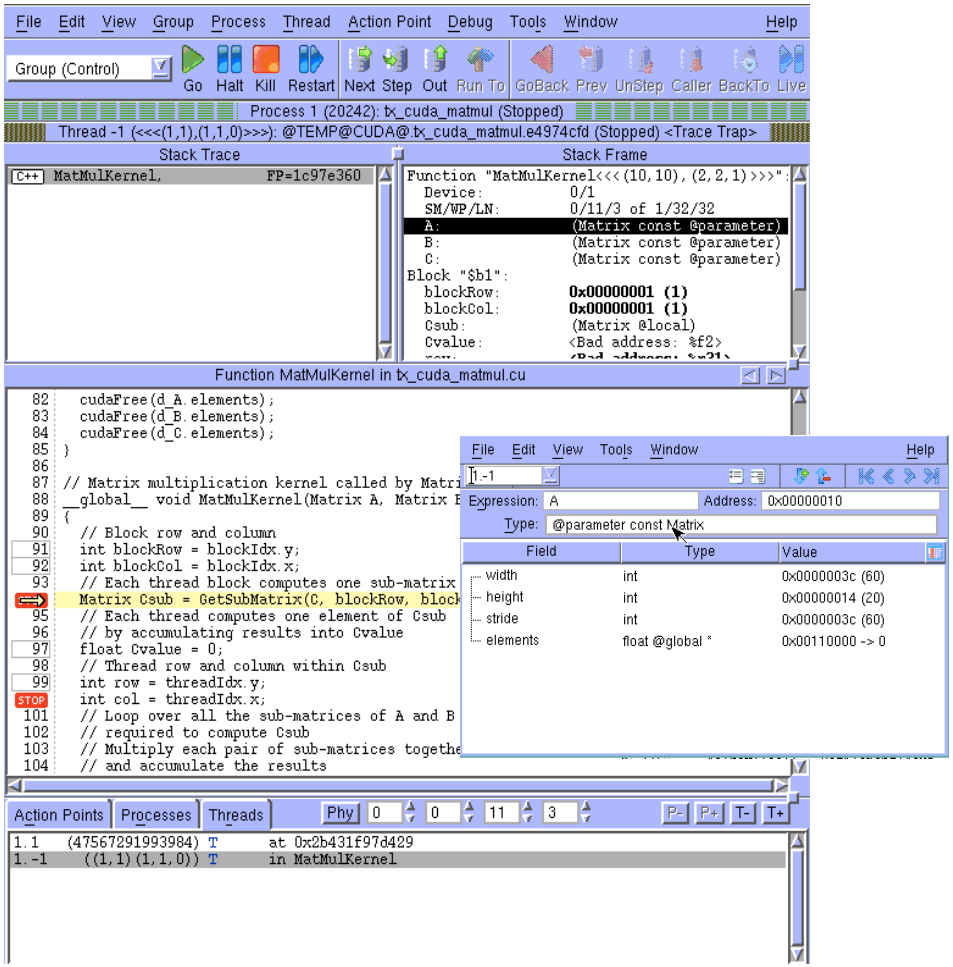
CUDA Port of TotalView



Debugging on the GPU device (not in an emulator)

Full visibility of both Linux and GPU threads

- Device threads shown as part of the parent Unix process
- Handles all the differences between the CPU and GPU

Fully represent the hierarchical memory

- Display data at any level (registers, local, block, global or host memory)
- Making it clear where data resides with type qualification

Thread and Block Coordinates

- Built in runtime variables display threads in a warp, block and thread dimensions and indexes
- Displayed on the interface in the status bar, thread tab and stack frame

Device thread control

- Warps advance synchronously

Handles CUDA function inlining

- Step into or over inlined functions
- Functions show on stack trace

Reports memory access errors

- CUDA memcheck

Multi-Device Support

Can be used with MPI

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Debugging CUDA applications

- **Applications can take advantage of**
  - Kernels execute asynchronously
    - Overlap of communication and computation
    - The same kernel can operate on multiple streams
  - Multi-process applications
  - Utilization of multiple GPUs at the same time
  - Multi-level parallelism
    - MPI + OpenMP + CUDA
- **Interface rapidly developing with each release of the SDK**
  - Rogue Wave is working closely with NVIDIA to take advantage of capabilities as they are introduced

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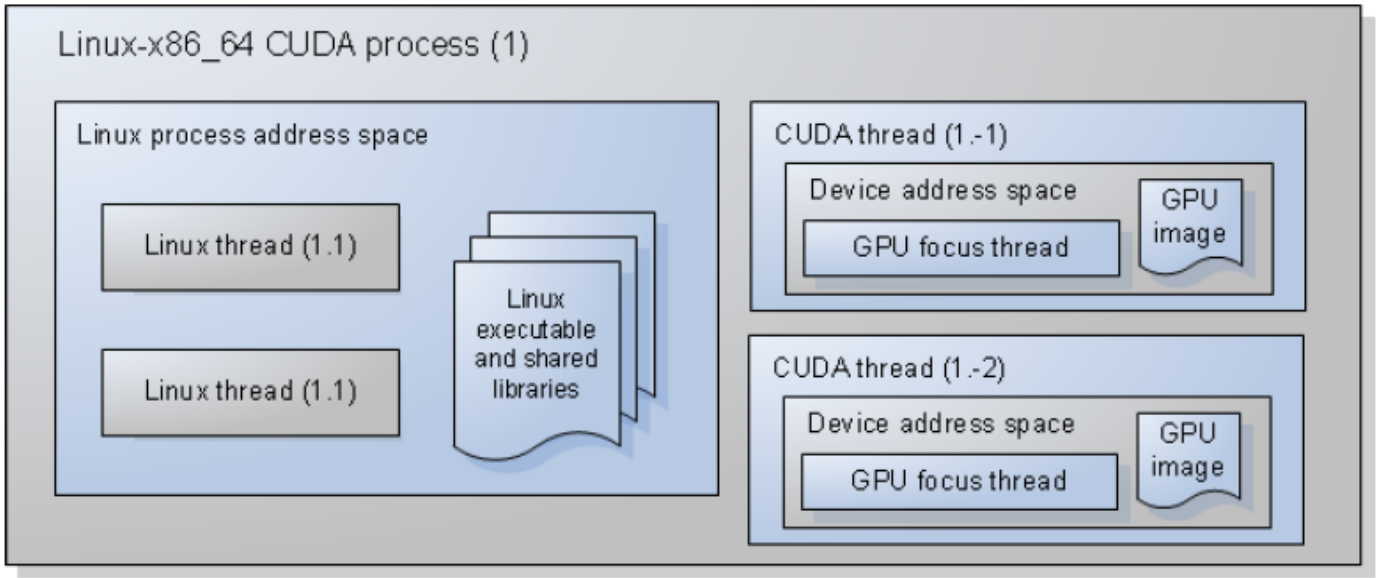
TotalView CUDA Debugging Model



- **A Linux-x86_64 CUDA process consists of:**
  - **A Linux process address space, containing:**
    - **A Linux executable and a list of Linux shared libraries.**
  - **A collection of Linux threads, where a Linux thread:**
    - **Is assigned a positive debugger thread ID.**
  - **A collection of CUDA threads, where a CUDA thread:**
    - **Is assigned a negative debugger thread ID.**
    - **Has its own separate address space**

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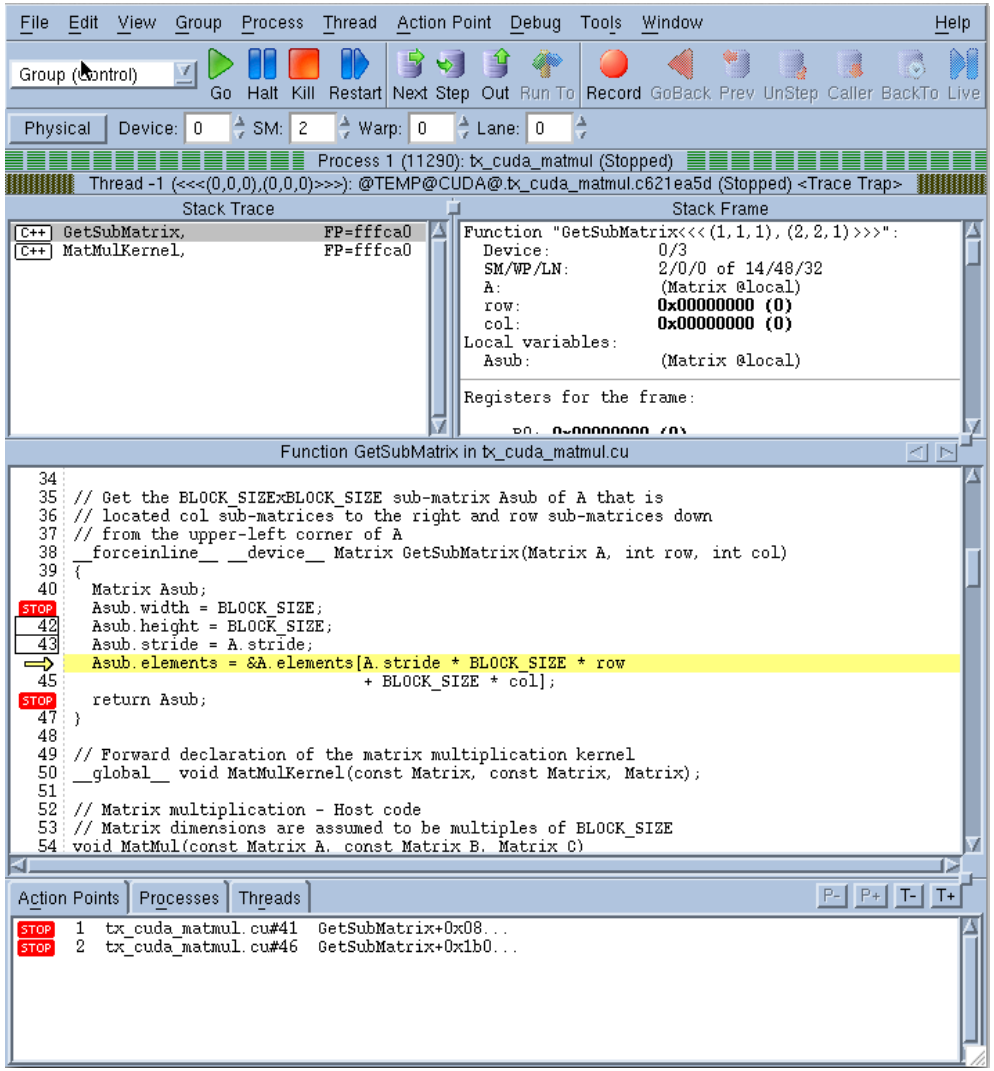
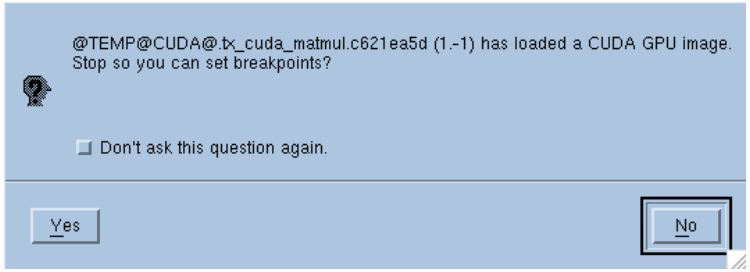
Starting TotalView





- Once a new kernel is loaded TotalView provides the option to stop and set breakpoints
- TotalView automatically configures the GUI for CUDA debugging
- Debugging CUDA code is done by using normal TotalView commands and procedures

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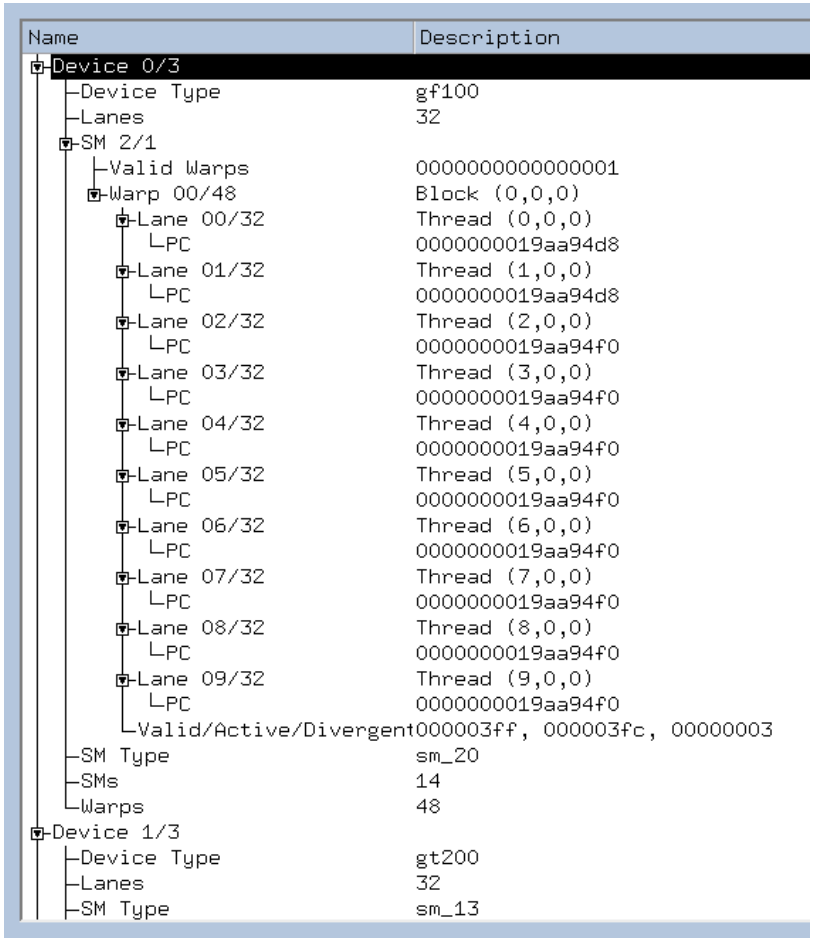
GPU Device Status Display

Provides the “high-level” view

- Values automatically update as you step through code
- Shows what hardware is in use
- Helps to map between logical and hardware coordinates



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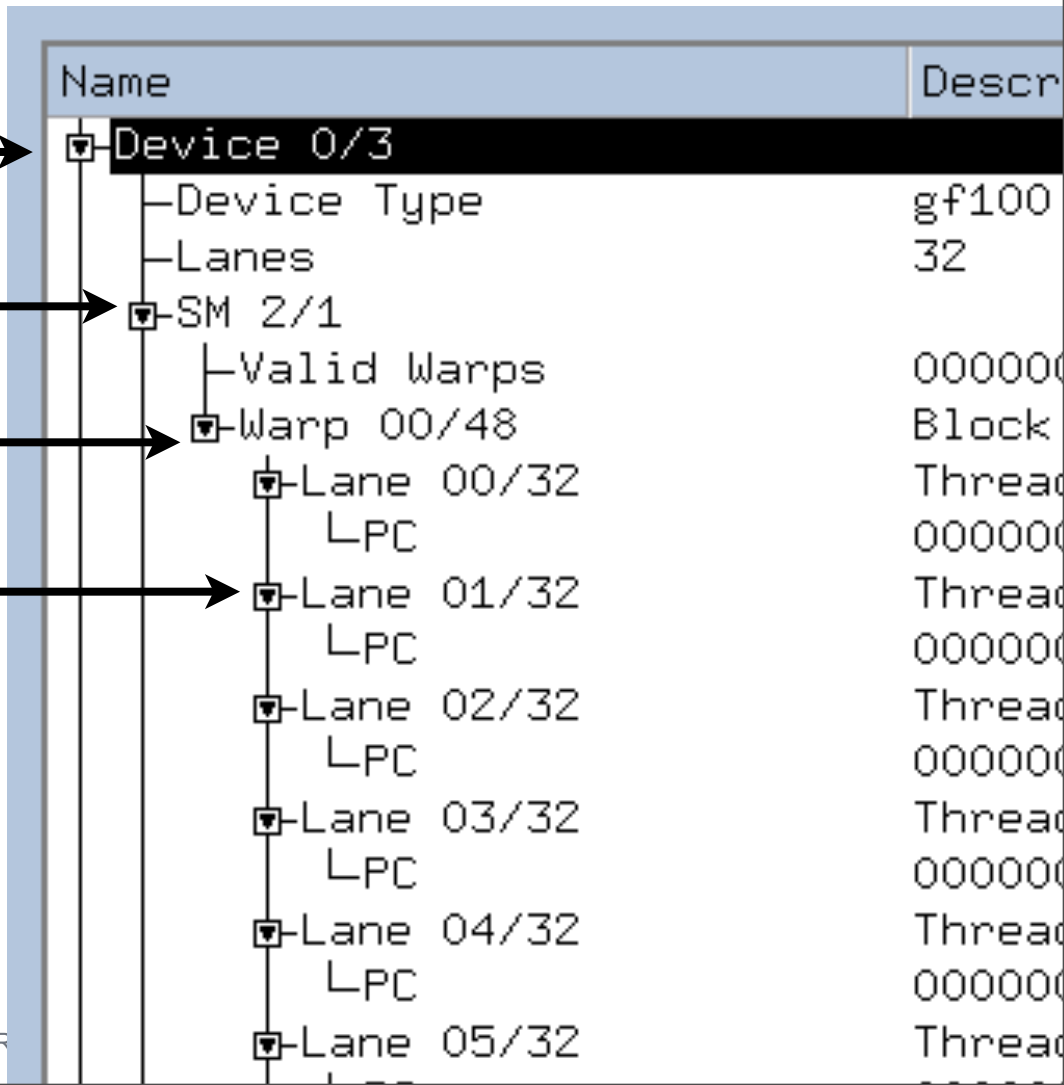
GPU Device Status Display

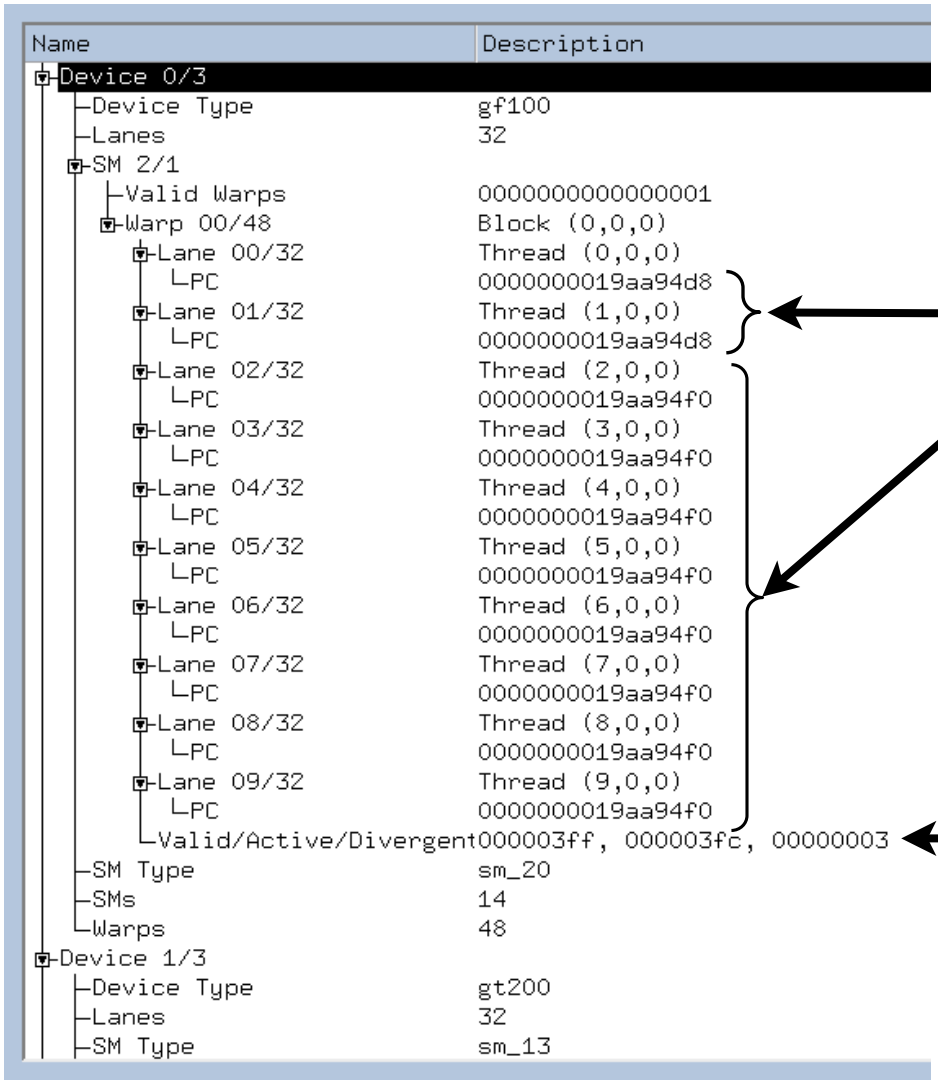
Provides detailed information for:

- Device and Type
- SMs
- Warps
- Lanes with PC



Information updates as you step

GPU Device Status Display



Name	Description
Device 0/3	
Device Type	gf100
Lanes	32
SM 2/1	
Valid Warps	0000000000000001
Warp 00/48	Block (0,0,0)
Lane 00/32	Thread (0,0,0)
PC	0000000019aa94d8
Lane 01/32	Thread (1,0,0)
PC	0000000019aa94d8
Lane 02/32	Thread (2,0,0)
PC	0000000019aa94f0
Lane 03/32	Thread (3,0,0)
PC	0000000019aa94f0
Lane 04/32	Thread (4,0,0)
PC	0000000019aa94f0
Lane 05/32	Thread (5,0,0)
PC	0000000019aa94f0
Lane 06/32	Thread (6,0,0)
PC	0000000019aa94f0
Lane 07/32	Thread (7,0,0)
PC	0000000019aa94f0
Lane 08/32	Thread (8,0,0)
PC	0000000019aa94f0
Lane 09/32	Thread (9,0,0)
PC	0000000019aa94f0
Valid/Active/Divergent	000003ff, 000003fc, 00000003
SM Type	sm_20
SMs	14
Warps	48
Device 1/3	
Device Type	gt200
Lanes	32
SM Type	sm_13

It also provides information for divergent GPU threads

Different PC for two groups of Lanes

State of Lanes inside the Warp

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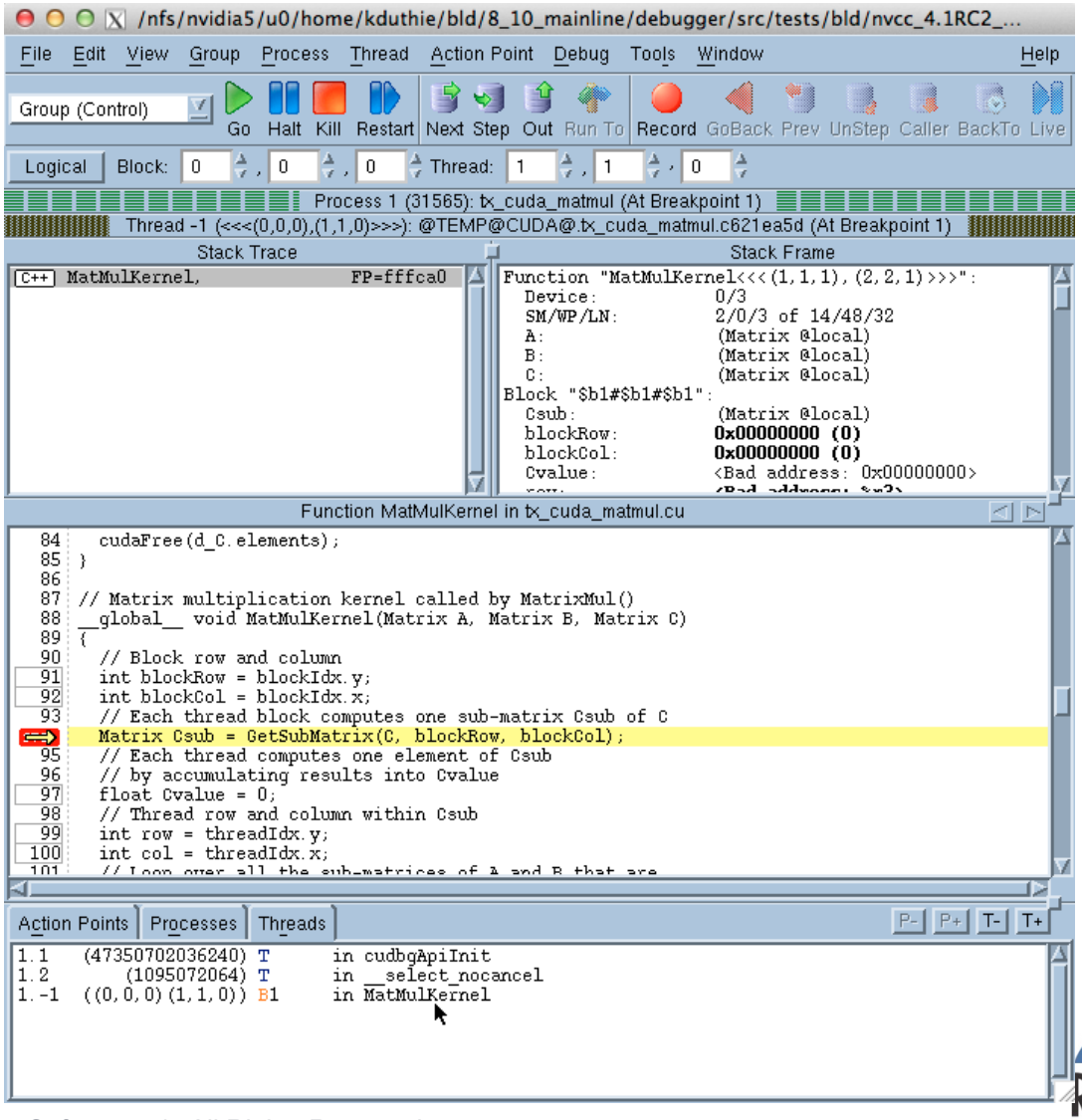
Debugging CUDA

Information on GPU execution, location and data is readily available.
... the same as it is for Linux processes and threads.



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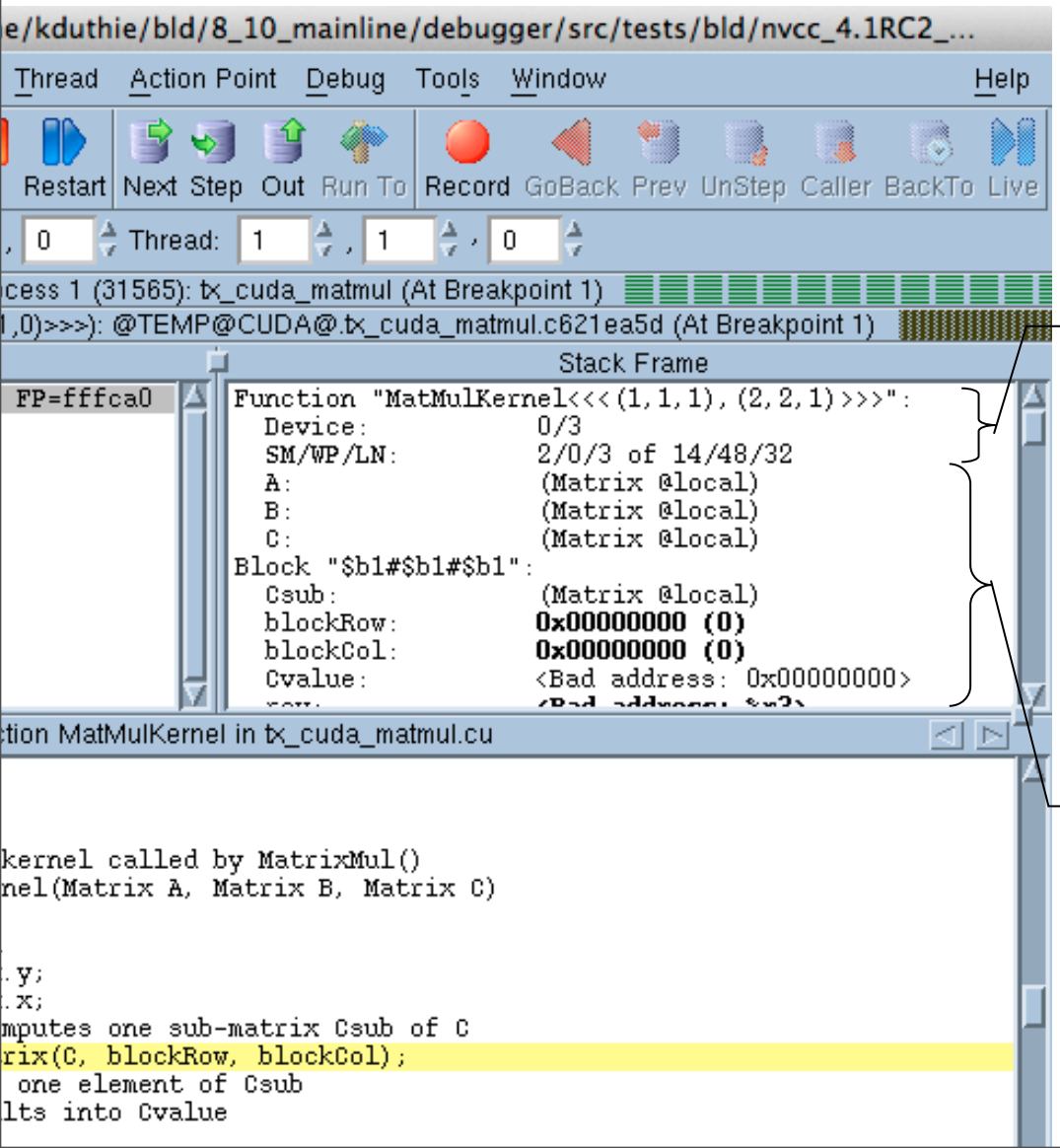
Debugging CUDA



CUDA grid and block dimensions, lanes/ warp, warps/SM,

Parameter, register, local and shared variables

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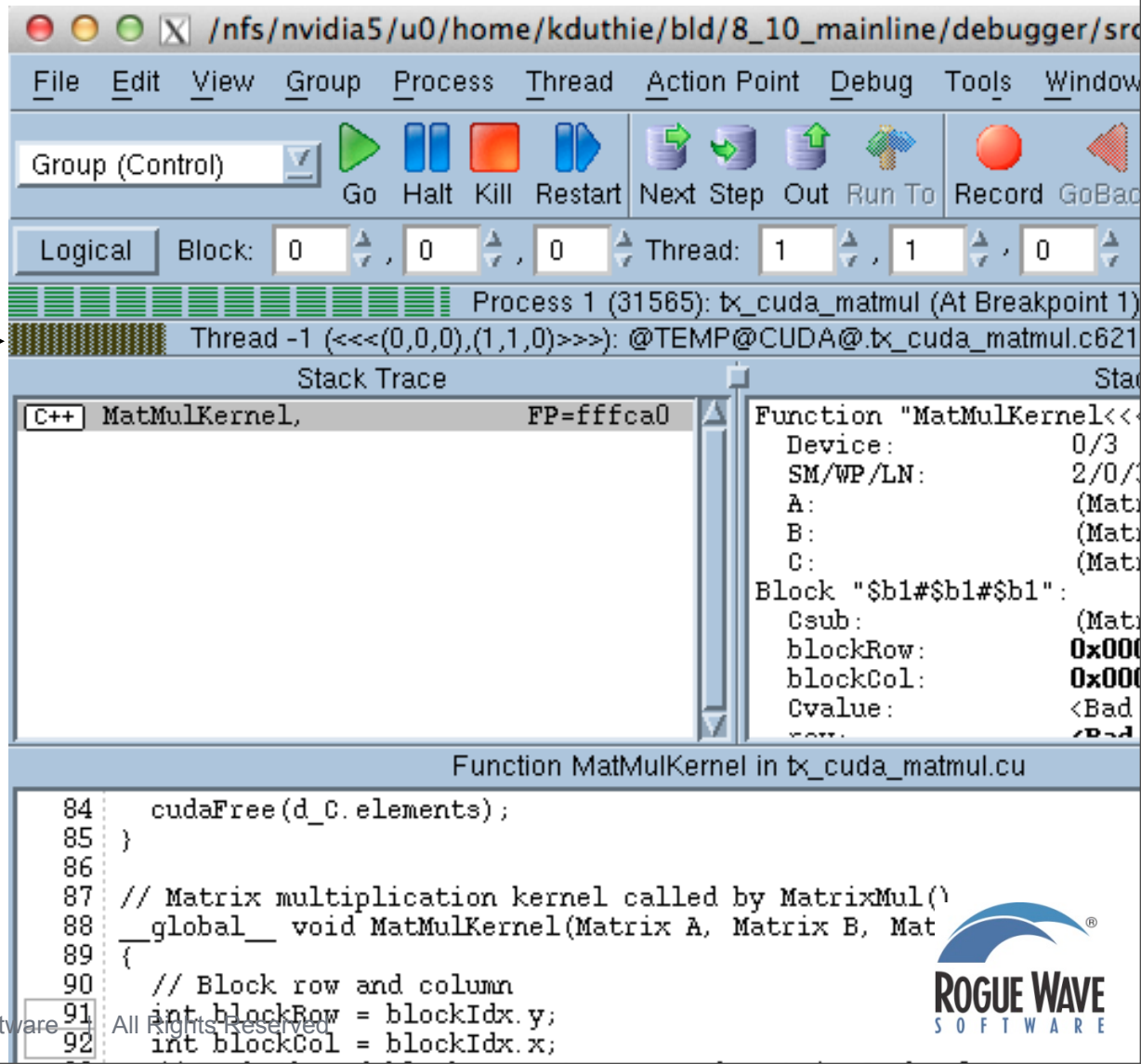
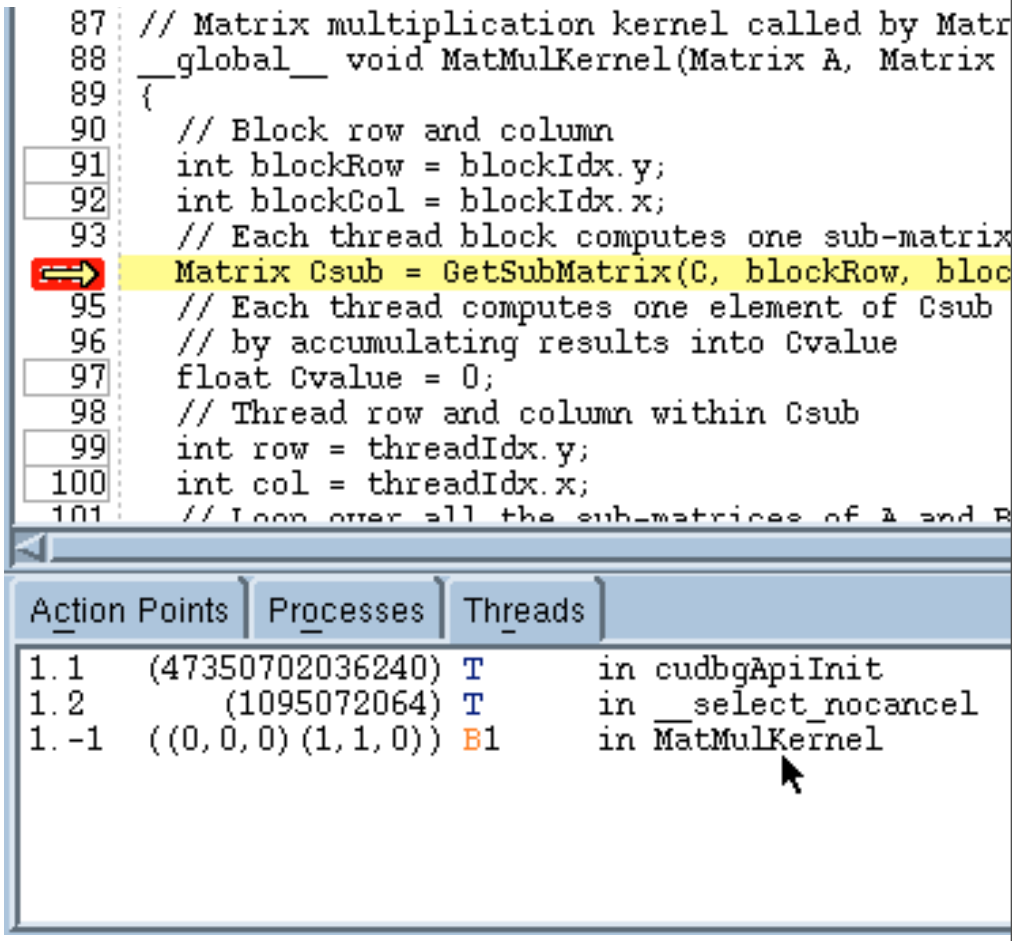
Debugging CUDA

GPU focus thread logical coordinates in the header...



Debugging CUDA

... as well as in the Process Window



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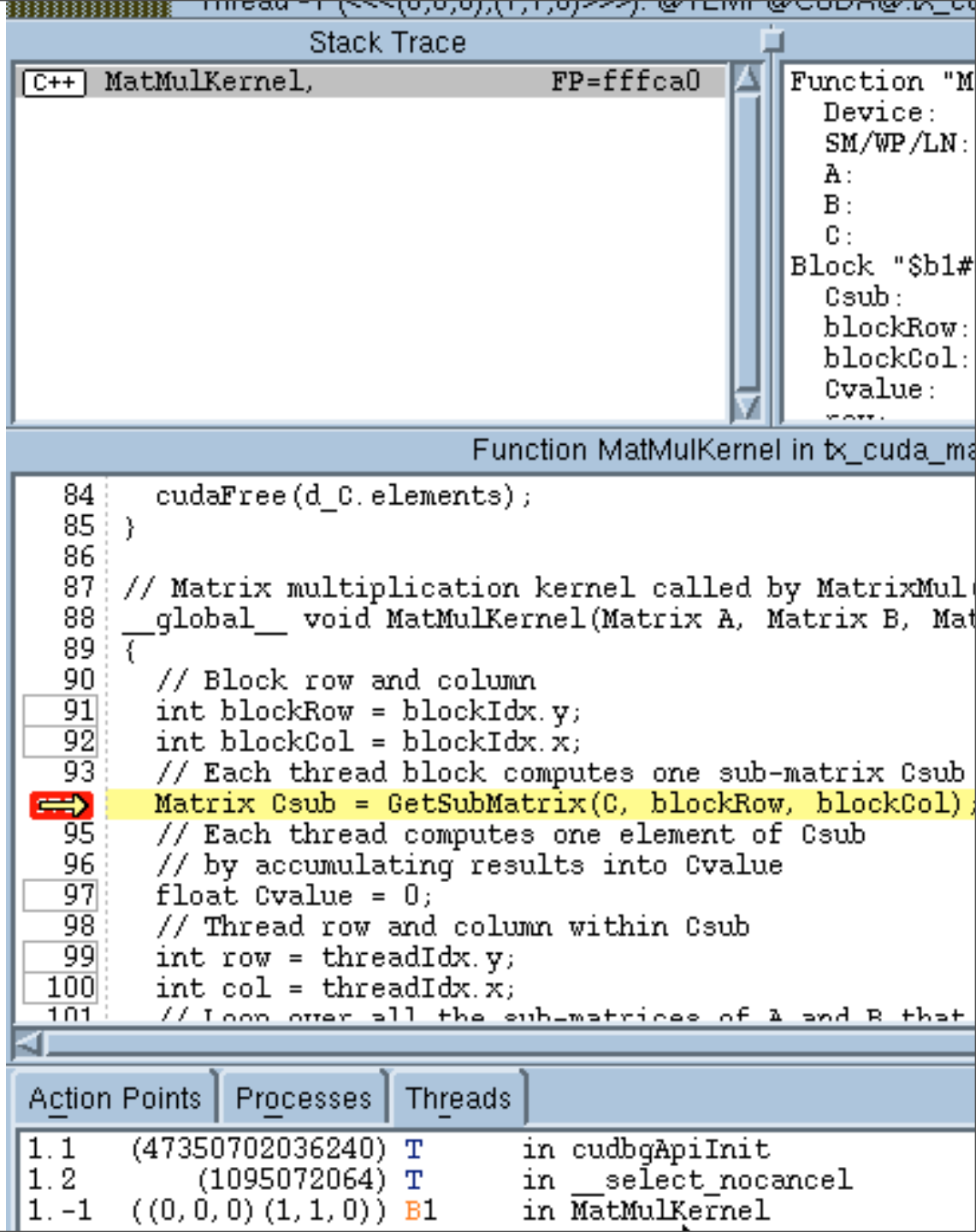
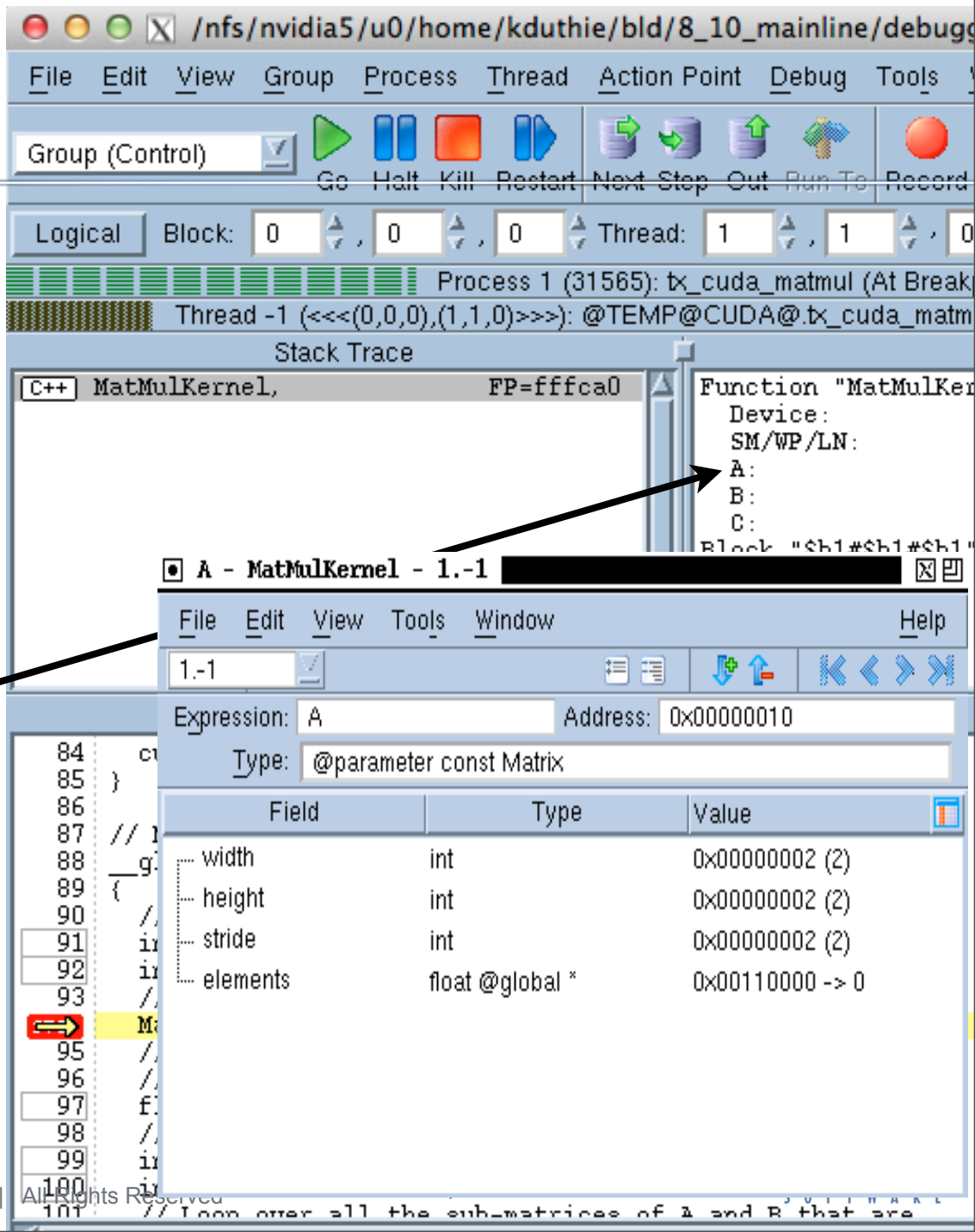
Debugging CUDA

PC arrow shows the Program Counter for the warp

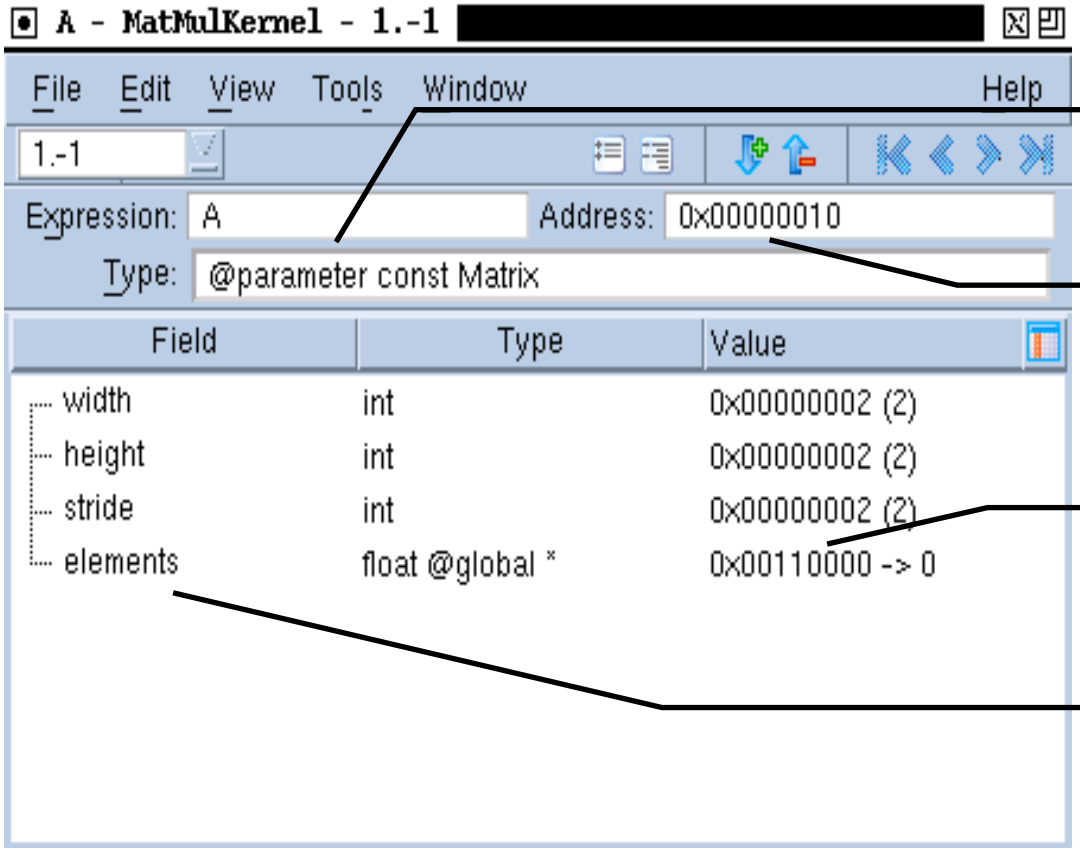


Debugging CUDA

Dive on any variable name to open a variable window



Debugging CUDA



"@parameter" type qualifier indicates that variable "A" is in parameter storage

Address 0x10 is an offset within parameter storage

Pointer value 0x110000 is an offset within global storage

"elements" is a pointer to a float in global storage

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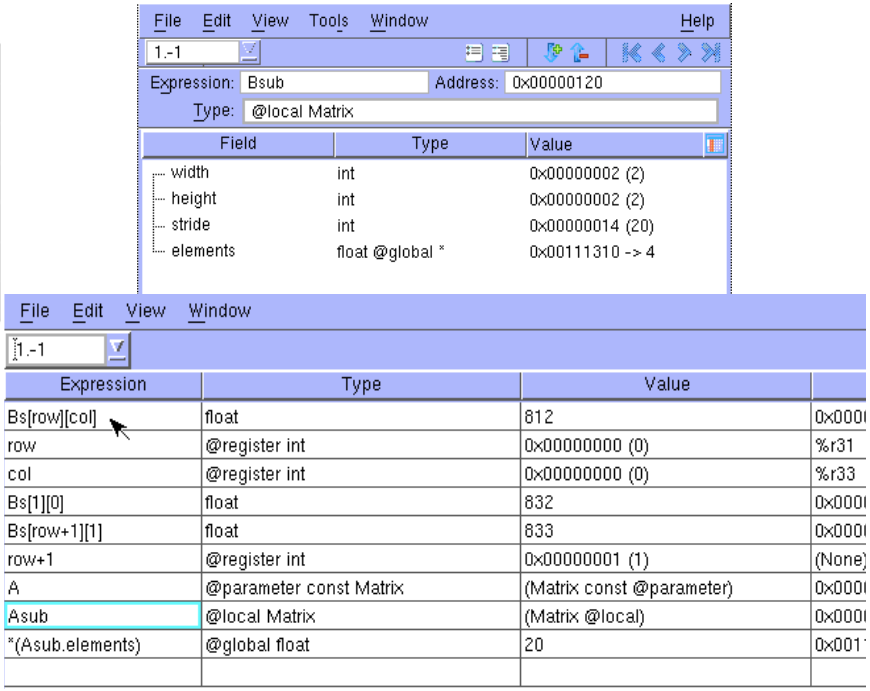
Storage Qualifiers

- **Denotes location in hierarchical memory**
  - Part of the type – using "@" notation
  - Each memory space has a separate address space so 0x00001234 could refer to several places

Storage Qualifier	Meaning
@parameter	Address is an offset within parameter storage.
@local	Address is an offset within local storage.
@shared	Address is an offset within shared storage.
@constant	Address is an offset within constant storage.
@global	Address is an offset within global storage.
@register	Address is a PTX register name



- **Used throughout expression system**
  - You can cast to switch between different spaces

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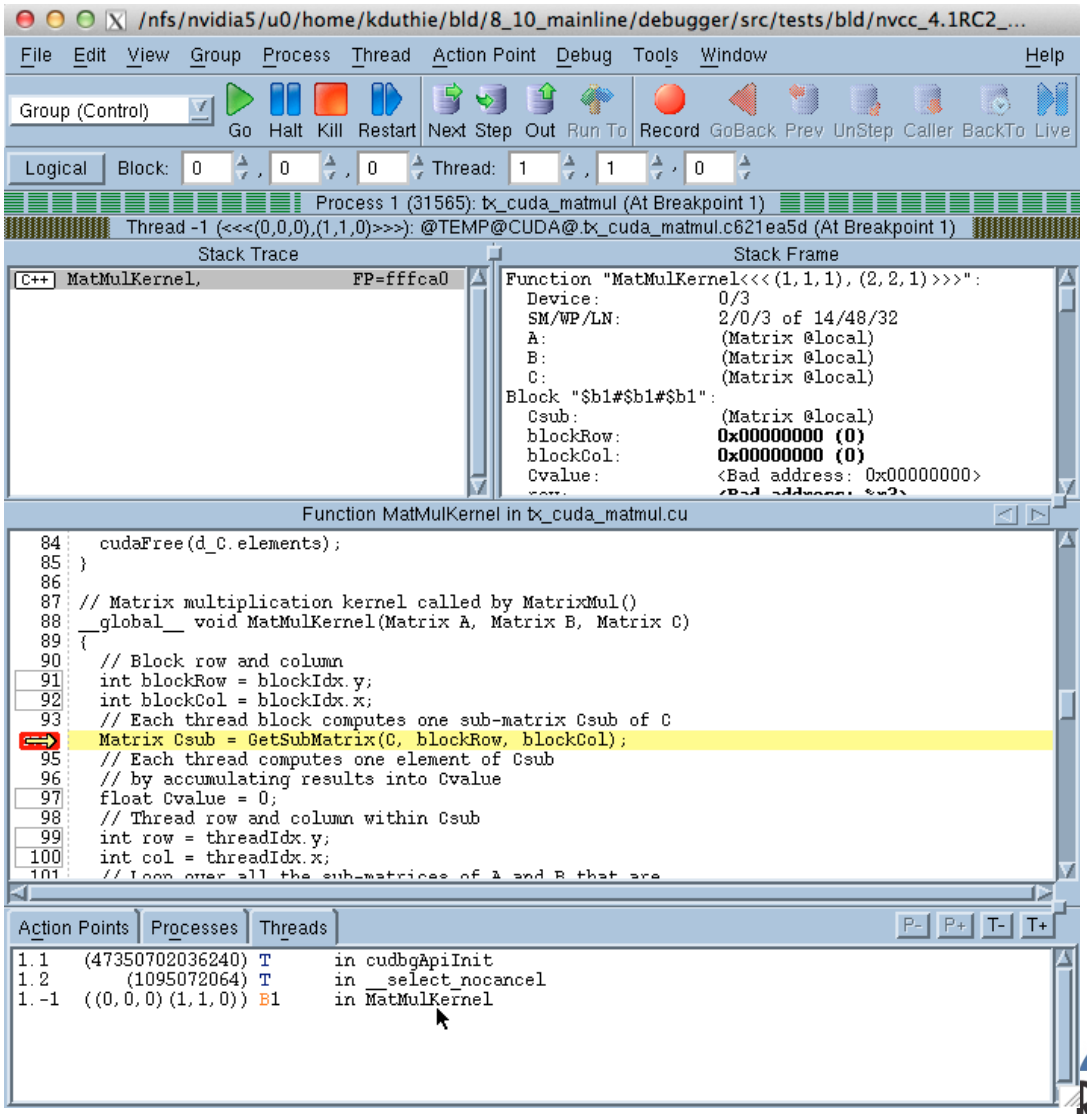
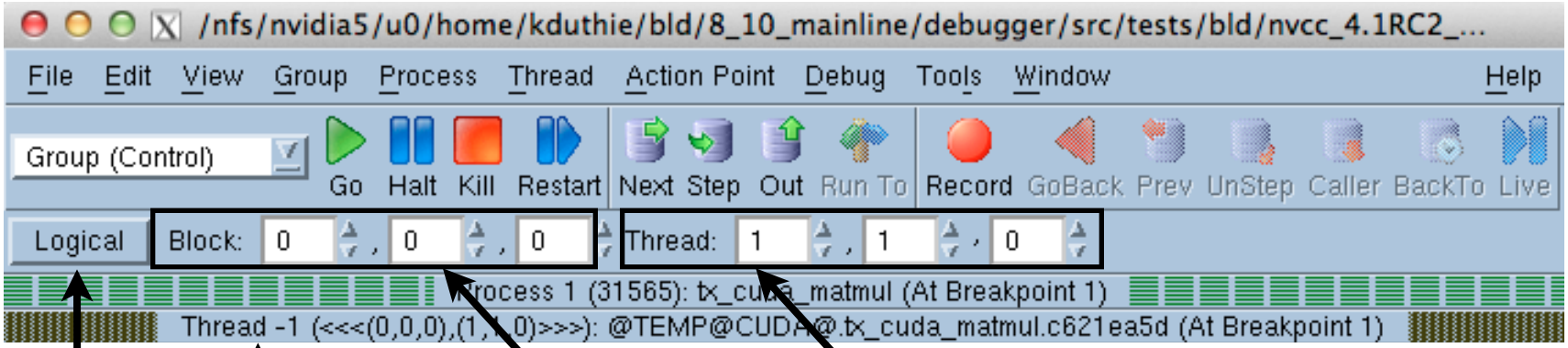
Debugging CUDA - Navigation

Navigate through your CUDA code in the Process Window as you wish...
Using either of two coordinate systems:



Debugging CUDA - Navigation



CUDA GPU threads have a negative TotalView thread ID

Block (x,y,z)

Thread (x,y,z)

User-controlled "spinboxes" allow selection and display of any part of your GPU execution

GPU focus thread selector for changing the logical block and thread indexes of the CUDA thread.

- **Logical: 2 or 3D Grid of Blocks, 3D Thread Within Grid**

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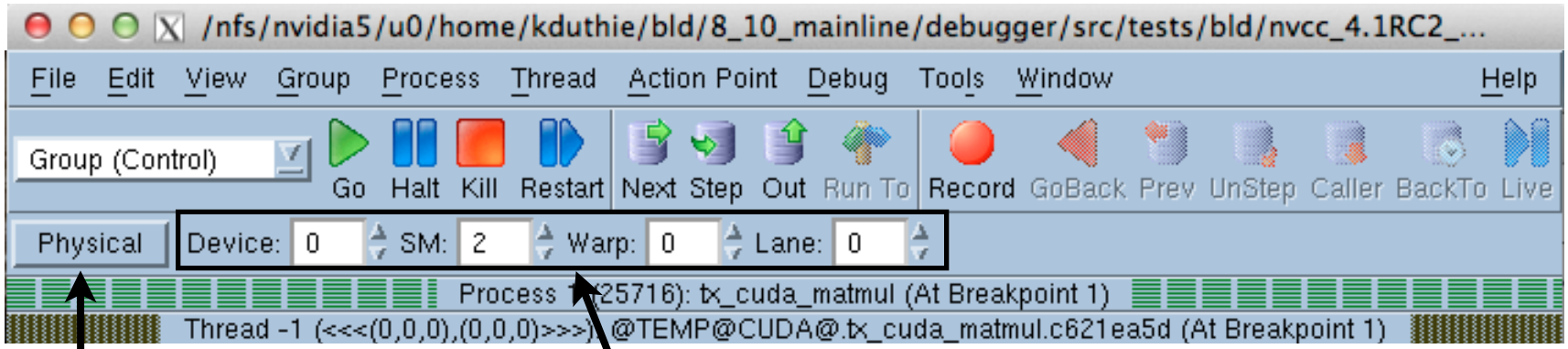
Debugging CUDA - Navigation



Device, SM, Warp, and Lane

User-controlled "spinboxes" allow selection and display of any part of your GPU execution

GPU focus selector for changing physical indexes of the CUDA thread.

- **Physical: Device, SM, Warp, Lane**

Executing GPU Code - Threads and Warps

Execution Control

- Single-step operation advances all of the GPU hardware threads in the *same* warp
- To advance the execution of more than one warp:
  - set a breakpoint and continue the process, or
  - select a line number in the source pane and select “Run To”.
- Warps advance synchronously
  - Warps share a PC
- Single stepping
  - Advances the warp containing the focus thread
  - Stepping over a __syncthreads() call advances all the relevant threads
- Halt
  - Stops all the host and device threads

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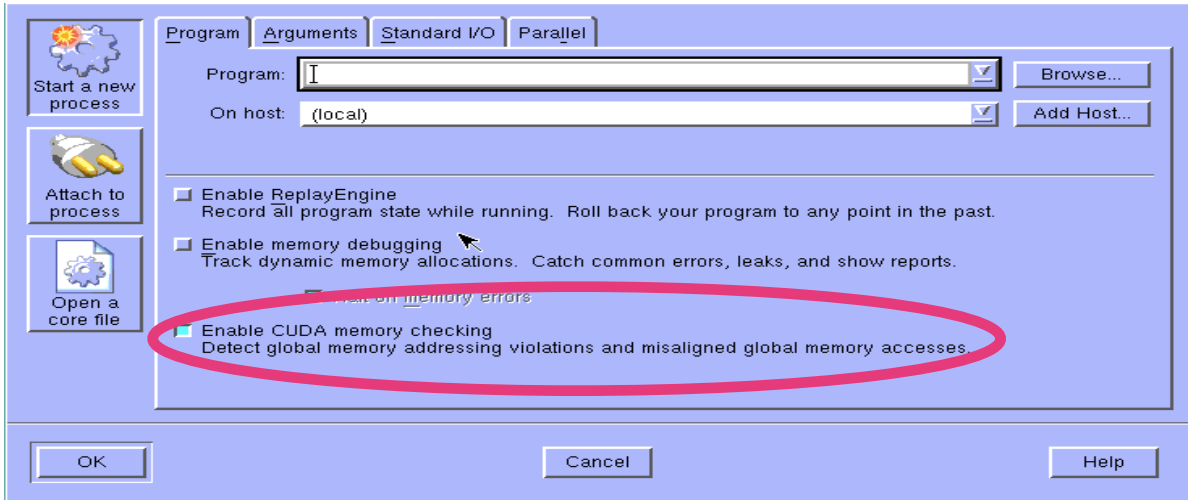
CUDA Segmentation Faults

- **TotalView displays segmentation faults as expected**
  - **Enable CUDA memory checking in New Program dialog window**



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TV 8.10 support for CUDA 4.1 specific features

- Works with the CUDA 4.1 SDK and Runtime
  - New Compiler Front End
  - Slight differences in the debug API
- Support for no copy pinned memory
  - This was broken at the driver level in 4.0
- New support for CUDA device assertions
- New support for multiple CUDA contexts from the same process on the same device
- Support for CUDA on the Cray XK environment

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OpenACC

- Pragma Based
  - Similar to OpenMP
  - Supports C and Fortran
- OpenACC Vendors
  - Cray
  - PGI
  - CAPS
- TotalView early access with Cray CCE 8
- Working with PGI and CAPS towards support

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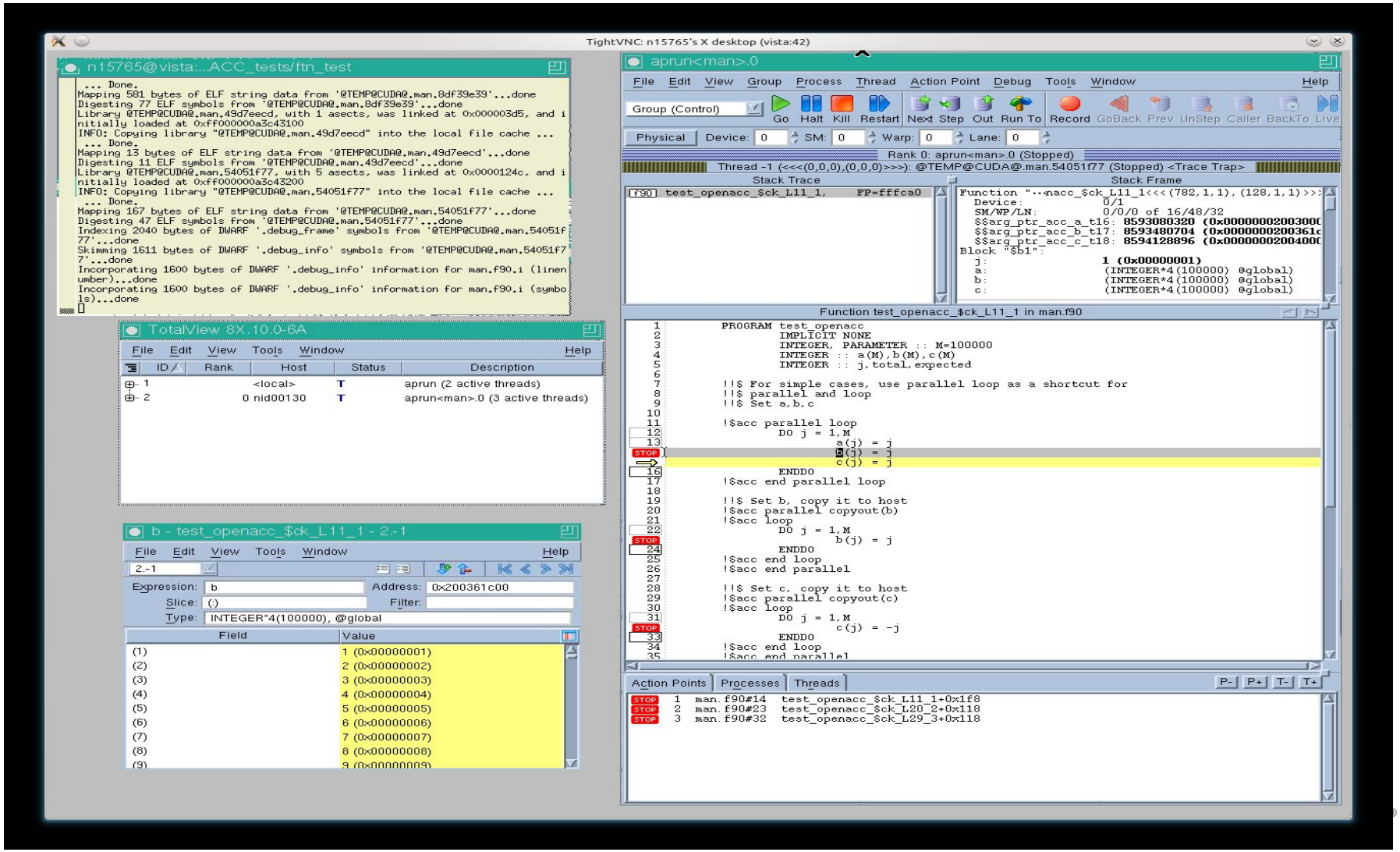
OpenACC



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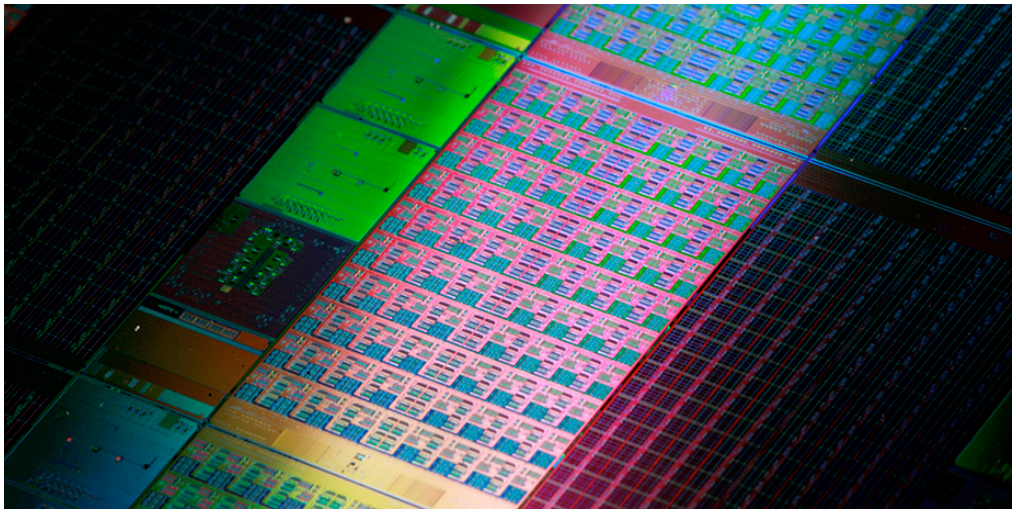
What's New

Intel Phi Debugging

with

TotalView



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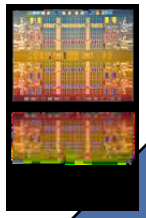
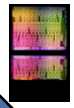
A Spectrum of Programming Use Models



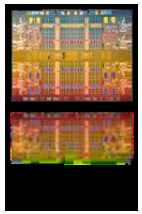


Xeon-Centric

MIC-Centric

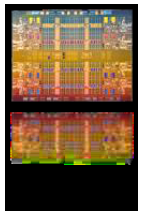
Xeon-native | Offload | Symmetric | Reverse Offload | MIC-native

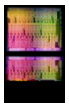
General Purpose Serial and Parallel Codes



Main()
MPI_
Foo()

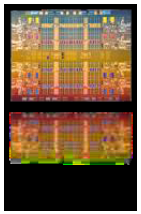
Scalar codes with highly parallel phases





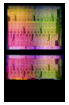
Main()
---
offload<MIC>
Foo()

Codes with balanced needs

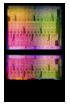


Main()
Foo()

Main()
Foo()

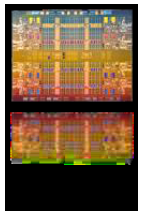


Parallel codes with scalar phases

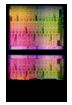


Main()

Offload<Xeon>
Foo()



Highly parallel codes



Main()
MPI_
Foo()

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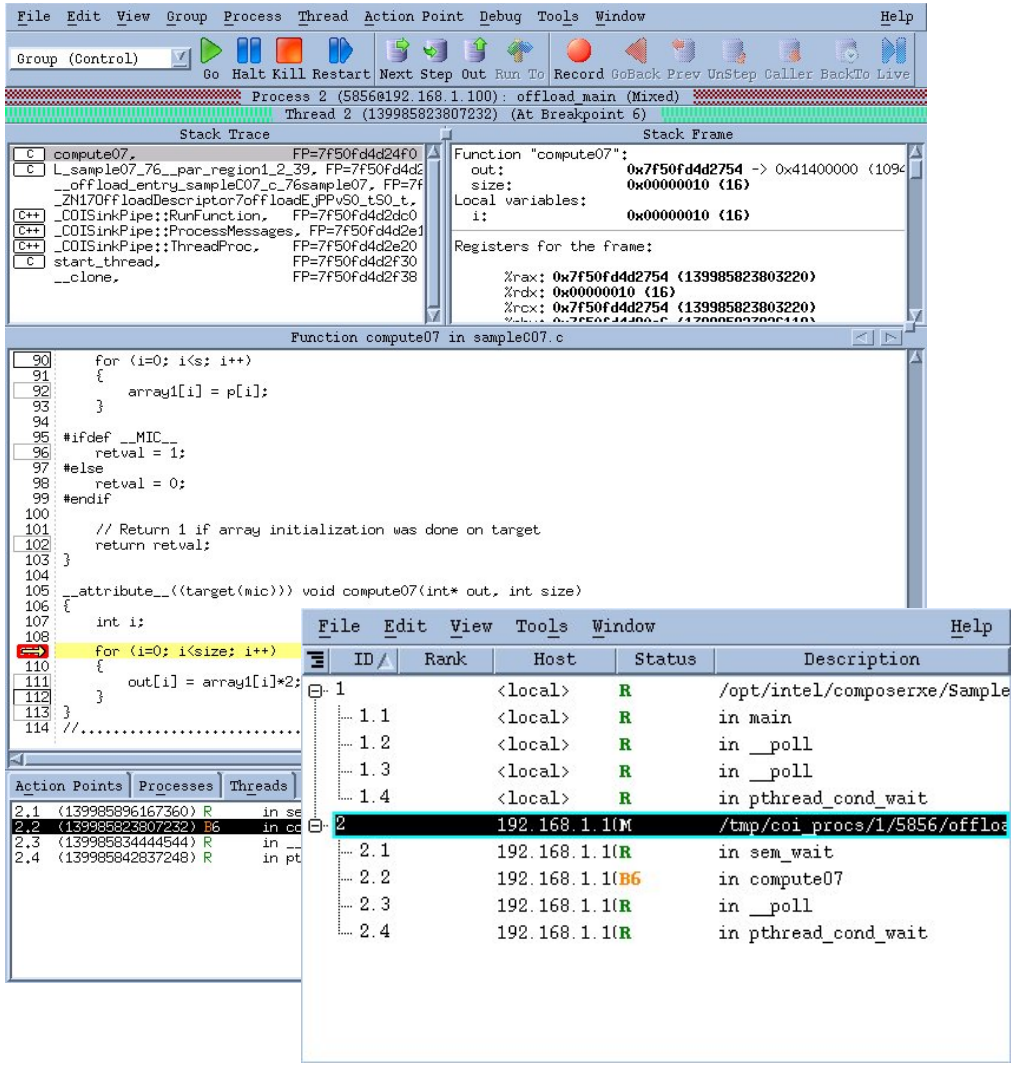
Intel MIC Port of TotalView



- **Full visibility of both host and Phi threads**
- **Full support of MPI programs**
- **Symmetric Debugging of heterogeneous applications with offloaded code**
- **Remote Debugging of Phi-native applications**
- **Asynchronous thread control on both Xeon and Phi**

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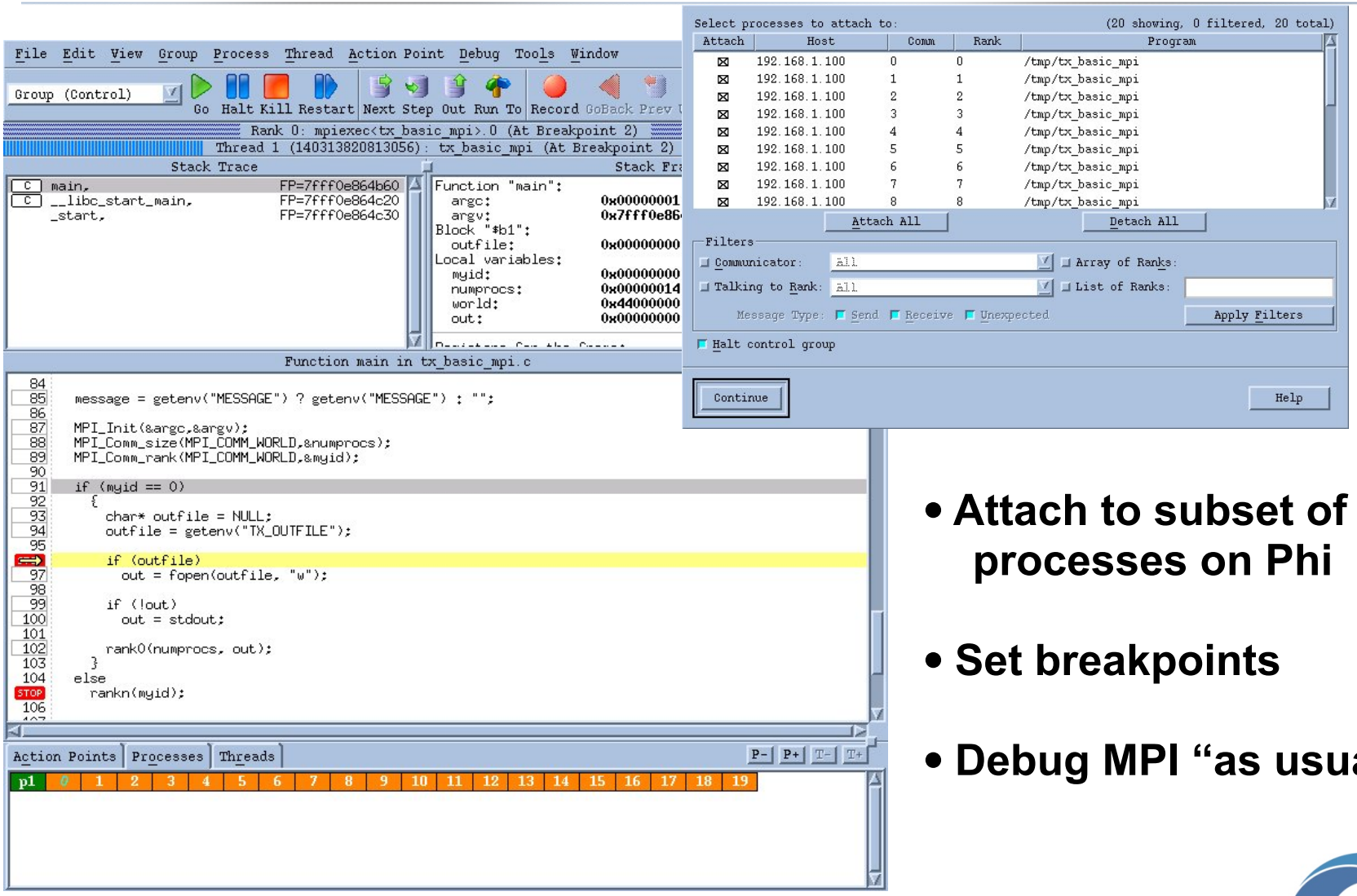
Debugging MPI Applications



- **Attach to subset of processes on Phi**
- **Set breakpoints**
- **Debug MPI "as usual"**

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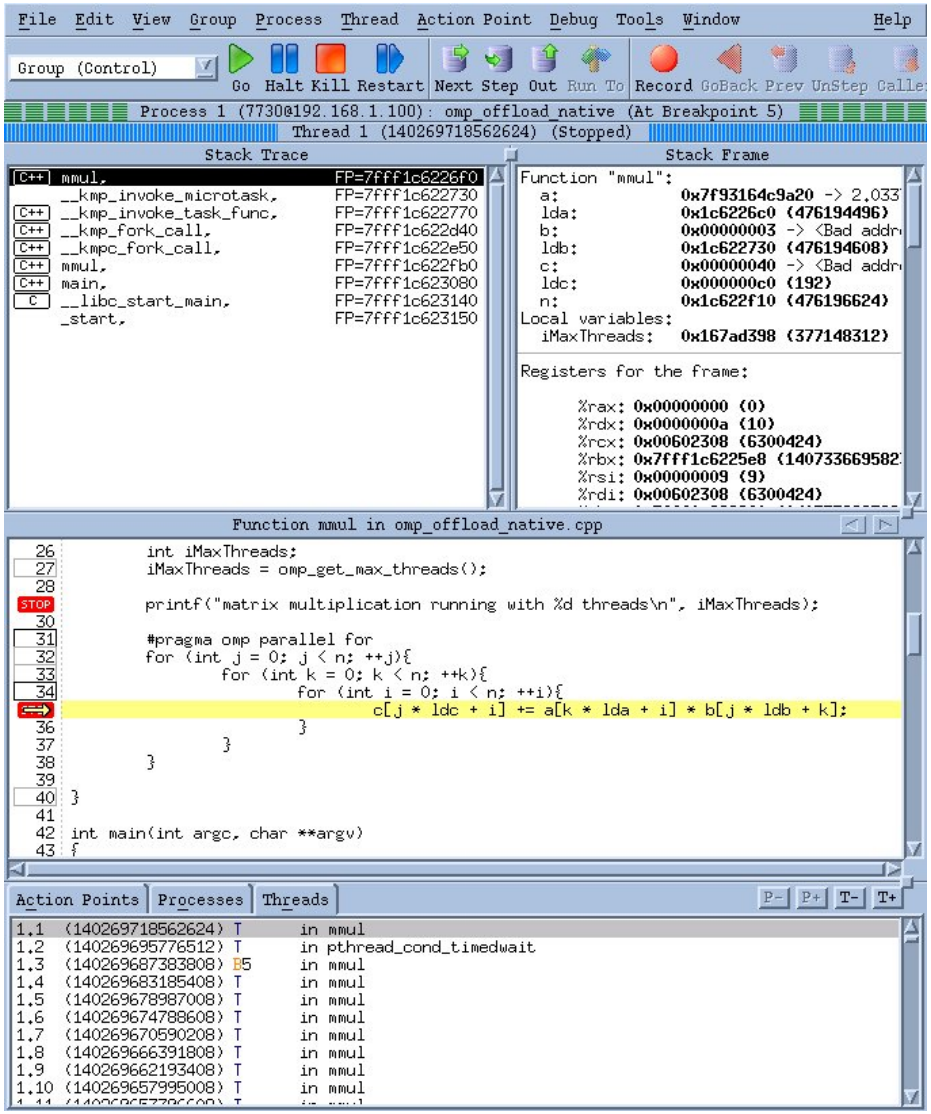
Remote Debugging of Applications on Phi



- Start application on Phi card
- Attach to running application
- See thread private data
- Investigate individual threads
- Kill stuck processes on Phi

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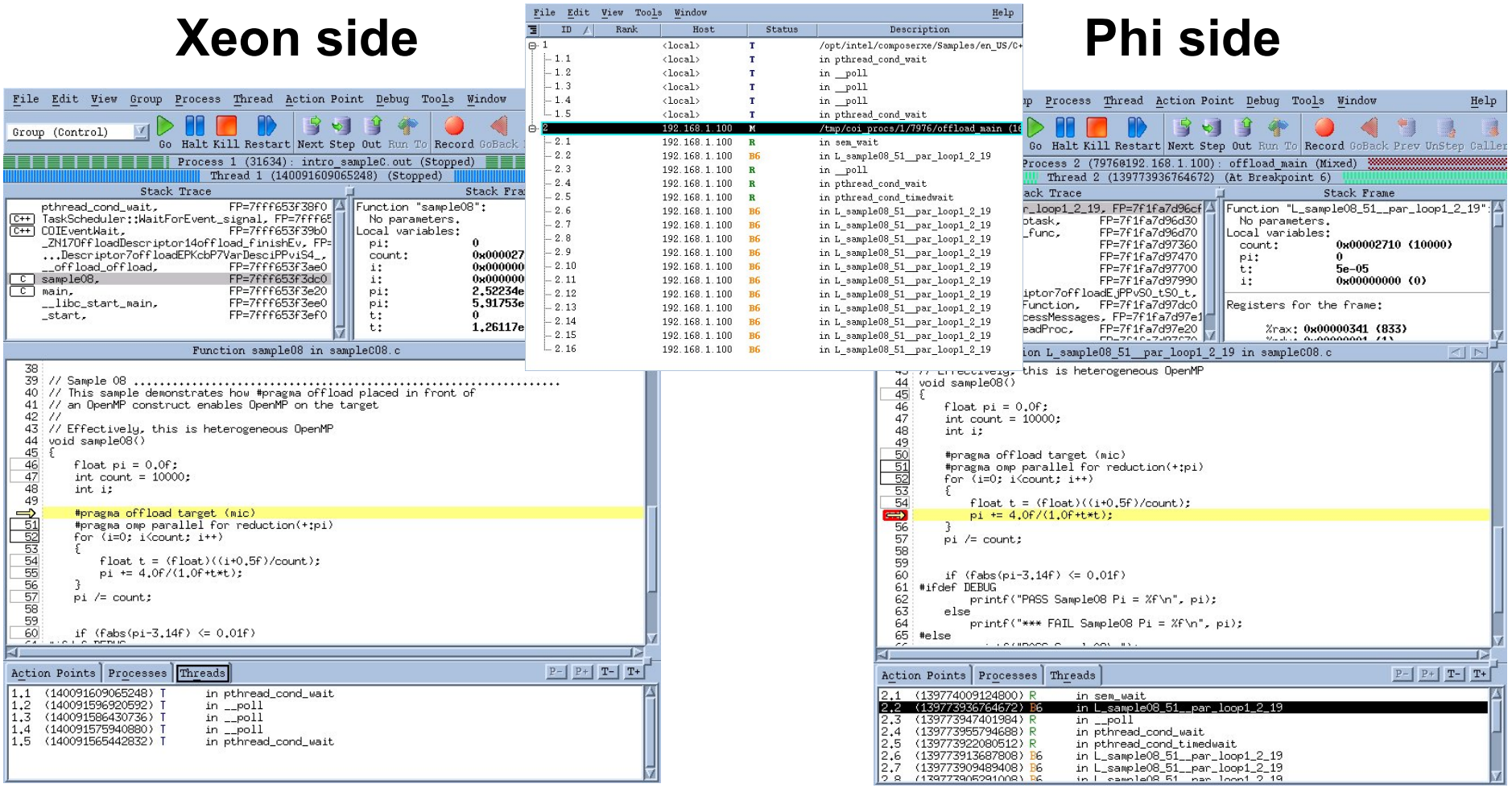
Debugging Applications with Offloaded Code

Xeon side

Phi side



One debugging session for Phi-accelerated code

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TotalView provides a full spectrum of debugging solutions

- **Code debugging**
  - Highly scalable interactive GUI debugger
  - Powerful features for debugging multi-threaded, multi-process, and MPI parallel programs
  - Compatible with wide variety of compilers across several platforms and operating systems
- **Memory Debugging**
  - Parallel memory analysis and error detection
    - Intuitive for both intensive and infrequent users
  - Easily integrated into the validation process
- **Reverse Debugging**
  - Parallel record and deterministic replay within TotalView
    - Users can run their program "backwards" to find bugs
  - Allows straightforward resolution of otherwise stochastic bugs
- **GPU CUDA Debugging**
  - Full Hybrid Architecture Support
  - Asynchronous Warp Control
  - Multi-Device and MPI Support
- **Intel Phi Debugging**
  - Multi-Model Support
  - Early Experience Program Available

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Summary, Conclusions, Next Steps and Questions

- Rogue Wave Software provides a suite of tools and libraries that can accelerate your software engineering efforts
- TotalView provides comprehensive hybrid debugging environment
- Initial support for Intel PHI has begun.
  - Including support for multiple workflows
  - We are interested in learning the workflows that you are going to apply
  - If you are interested in our early experience program, let us know.
- Questions?

ROGUE WAVE SOFTWARE

Thanks!

Thank You

Download a TotalView evaluation at:

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